Description

Sensor arrangement and method for operating a sensor arrangement

The invention relates to a sensor arrangement and a method for operating a sensor arrangement.

The interface between biology and semiconductor technology is of interest from scientific and economic standpoints. Mention may be made in this connection of, by way of example, the coupling between biological cell assemblages, such as neurons for example, and silicon microelectronics. A biological system may be examined in spatially or temporally resolved fashion on the surface of a semiconductor-technological sensor by means of sensor elements arranged in matrix form. In particular, metabolism parameters of the cells can be recorded for example by detecting local pH values with the aid of ion-sensitive field-effect transistors (ISFETs) as sensor elements. An ISFET has an ion-sensitive layer in operative contact with electrically charged particles to be detected, the electrically charged particles characteristically influencing the conductivity of the ISFET, which can be detected as a sensor variable.

Examining the reaction of a biological system to an electrical stimulation is of great interest. Neurons (nerve cells) can generate a small electric current via ion channels in the cell membranes in specific regions of their surface, said current being detected by a sensor situated underneath. The requisite stringent requirements made of spatial and temporal resolution of the sensor are achieved by means of silicon microelectronics.

Matrix-type arrangements of sensor elements are also

used in other important fields such as medical analysis or DNA sensor technology.

For these and other possible applications of semiconductor sensors in integrated circuits, it is advantageous to integrate a large number of sensors in a common sensor array. Even in the case of small sensor arrays (and all the more so in the case of large sensor arrays), not every sensor can be connected to a dedicated read-out circuit. The number of requisite lines and also the redundancy of the read-out circuits arranged outside the array are factors opposing such a solution.

Figure 1 schematically shows a sensor arrangement 100 in accordance with the prior art having four sensor devices 101 to 104, a multiplexer represented as switch 105, and a read-out circuit 106.

The outputs of the individual sensor devices are read out using the multiplexer 105, that is to say serially. The respective sensor device 101 to 104 coupled to the read-out circuit 106 via the multiplexer 105 outputs an output voltage correlated with the event to be detected (for example the illumination intensity in the case of a photosensor or an electrical signal of a nerve cell arranged on the respective sensor device). In order to represent these facts schematically, the sensor devices 101 to 104 are represented schematically as voltage sources V_1, V_2, V_3, V_4.

In accordance with the scenario illustrated in figure 1, the first sensor device 101 is coupled to the read-out circuit 106 via the multiplexer 105. By means of the read-out circuit 106, the output voltage of a respective sensor device 101 to 104 is amplified for further processing.

If it is necessary to record the measured values of a multiplicity of sensor devices with a high sampling rate, then an individual sensor device has to be read in a very short time. This results in a stringent
5   requirement made of the temporal resolution of the system.

The sensor arrangement 200 in accordance with the prior art as shown in **figure 2** exhibits, in addition to the
10   components described in figure 1, an internal resistance R_i 201 of each of the sensor devices and also a common capacitance C 202 of the sensor devices 101 to 104. The time constant of the sensor arrangement 200 is determined by means of the RC element comprising
15   internal resistance R_i of the sensor devices 101 to 104 and also the capacitance C 202 that is to be subjected to charge reversal. These two parameters are subject to specific limitations for a specific production technology. Consequently, the achievable time constant
20   τ = RC is also limited.

The time constant τ clearly specifies the time after which the output signal has risen to (1-1/e) = 63% of the final value. If measurement errors caused by the
25   transient response of the sensor arrangement 200 are intended to lie below a specific, just still tolerable limit, it is necessary, under certain circumstances, to wait during multiples of these time constants (e.g. 2τ or 3τ). Consequently, the time constant τ = RC is a
30   characteristic measure of the minimum time that can be attained between two successive measurements. Therefore, the value of τ results in a limitation of the maximum number of sensor devices that can be read within a predetermined time segment at a predetermined
35   sampling rate.

Figure 3 is a diagram 300 schematically showing the time dependence of the signal profile at a sensor

device 201 to 204 after the production of the coupling
(t = 0) of the respective sensor device to the read-out
circuit 106 via the multiplexer 105.

5   The time that has elapsed since the changeover of the
multiplexer 105 (t = 0) is plotted along the abscissa
301 of the diagram 300. At the instant t_0, the signal
profile has for the first time fallen below the
predetermined tolerable value V_{tol}. The temporal signal
10 profile at the voltage sources V_1 to V_4 represented
schematically in figure 1, figure 2, is represented
along the ordinate 302 of the diagram 300. The signal
profile curve 303 reflects the transient response at
the capacitance 202 and the resistances R_i, and to a
15 good approximation is a falling exponential function.
Clearly, at the instant t_0, the dynamic error has for
the first time fallen below the tolerable error, so
that the measurement time that is necessary at the
least is t_0.

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In the case of sensor arrangements disclosed in the
prior art, the sensor devices of a sensor array are
read in the voltage domain, that is to say that the
measurement variable is converted into an electrical
25 voltage. In order to keep down the RC constant, and
therefore to enable sufficiently many sensor devices to
be read sufficiently rapidly, attempts are made to
reduce the internal resistance R_i and, as a consequence
thereof, the time constant τ.

30

One possibility for reducing the internal resistance R_i
of the sensor devices independently of the circuit
architecture is to increase the driver capability of
the output transistors of a circuit. The disadvantage
35 of this measure is an increased area requirement and a
greater capacitive loading on the preceding amplifier
stage or the connected sensor, which leads to an
attenuation of the signal. On account of the frequently

severe area limitation and the need for efficient area utilization, this solution is not suitable for many fields of application.

5   Usually, for integrated circuits operated in the voltage domain, a series of basic circuits are used for the output drivers. What is disadvantageous about an additional output driver circuit integrated into the sensor devices is the increase in the space requirement

10   of a sensor device and, consequently, the reduction of the achievable spatial resolution. A boundary condition for the consideration below is that an output transistor coupled to a sensor electrode is simultaneously used for signal amplification. This is

15   not a mandatory prerequisite, however.

Figure 4A illustrates an output driver circuit 400, in the case of which a MOS transistor 401 is operated in a common-source connection.

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The sensor device is represented as voltage source V_G 402. Furthermore, the output driver circuit 400 is shown with a constant-current source I_0 403, a nonreactive resistance R 404 representing the internal

25   resistance of the sensor device, and also a capacitance C 405 representing the capacitance of a sensor arrangement. The output voltage V_{out} is present across the capacitance 405. The voltage source 402 is coupled to the gate terminal of a MOS transistor 401. One

30   source/drain terminal of the MOS transistor 401 is at ground potential 407, whereas the other source/drain terminal of the MOS transistor 401 is coupled both to the constant-current source 403 and to the nonreactive resistance 404 and to the capacitance 405. The

35   operating point of the MOS transistor 401 is determined by means of the constant-current source 403, the nonreactive resistance 404 and the voltage source V_G 402.

Figure 4B shows a small-signal equivalent circuit diagram 410 of the output driver circuit 400 shown in figure 4A. The equivalent circuit diagram 410 shows a controlled current source 411 ($g_m\Delta V_G$), an effective internal resistance 412 $(g_{ds}+R^{-1})^{-1}$ and also the capacitance 405 that is to be subjected to charge reversal. g_{ds} designates the output conductance of the MOS transistor 401, and g_m is the transconductance of the MOS transistor 401.

In the case of the common-source connection of the MOS transistor 401 as shown in figure 4A, figure 4B, one source/drain terminal is at ground potential 407. The operating point of the output driver circuit 400 is predetermined by means of the DC component of the voltage source V_G 402 at the gate terminal of the MOS transistor 401 and by means of the constant-current source I_0 with the internal resistance R coupled to the other source/drain terminal of the MOS transistor 401. A solution without a constant-current source I_0 403, just with a nonreactive resistance R 404, is also possible as an alternative. In the case of the output driver circuit 400 shown in figure 4B, a supply voltage 406 is applied to a respective terminal of the constant-current source 403 and of the nonreactive resistance 404, whereas a terminal of the voltage source 402, one source/drain terminal of the MOS transistor 401 and a terminal of the capacitance 405 are at ground potential 407.

If the gate voltage V_G is modulated (for example on account of a sensor event), then the drain current I_D of the MOS transistor 401 changes by $g_m\Delta V_G$. This is symbolized by means of the controlled current source 411 from figure 4B, showing the small-signal equivalent circuit diagram of the output driver circuit 400. The change in the output voltage ΔV_{out} results from the

changed voltage drop across the MOS transistor 401 and across the effective resistance 412. For low frequencies ω, the capacitance C can be disregarded to a good approximation, and this results in an open-loop gain $A(\omega=0)$ which can be described by means of the following expression:

$$A(\omega=0)=\Delta V_{out}/\Delta V_G=g_m/(g_{ds}+R^{-1}) \qquad (1)$$

If transistor parameters that are typical of CMOS technology are inserted into equation (1), this results in a possible voltage gain by a factor of approximately ten to approximately fifty. As a result, even signals having a small amplitude are amplified after the first amplifier stage such that they are no longer appreciably disturbed by noise effects. The time constant τ_c of the amplifier results as:

$$\tau_c=C/(g_{ds}+R^{-1}) \qquad (2)$$

The capacitance is predetermined by the technology used and, in this respect, can only be influenced to a very limited extent, for example by means of optimizing the layout. The parameters R and g_{ds} cannot be varied arbitrarily for a specific gain and on account of area limitations, so that a limit value for the maximum bandwidth that can be transmitted results from these boundary conditions.

A description is given below, referring to figure 5A, of a further output driver circuit 500 in accordance with the prior art. An equivalent circuit diagram 510 of the output driver circuit 500 shown in figure 5A is described referring to figure 5B. Those components of the output driver circuit 500 which are also contained in the output driver circuit 400 are provided with the same reference numerals.

In the case of the output driver circuit 500 shown in **figure 5A**, the MOS transistor 401 is configured in a source follower connection. In a departure from the output driver circuit 400 shown in figure 4A, that

5 source/drain terminal of the MOS transistor 401 which is not coupled to the constant-current source 403, the voltage source 402 and the capacitance 405 is at the potential of the supply voltage 406. Furthermore, a terminal of the constant-current source 403 and a

10 terminal of the capacitance 405 are at the electrical ground potential 407 in the case of the output driver circuit 500. The constant-current source I_0 403 and the voltage source V_G 402 determine the operating point of the MOS transistor 401.

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The electric current at the source/drain terminal of the MOS transistor 401 that is coupled to the constant-current source I_0 403 is determined by means of the constant-current source I_0 403. The gate voltage of the

20 MOS transistor 401 is set by means of the voltage source V_G 402. Furthermore, a capacitance C 405 that is to be subjected to charge reversal is shown.

The small-signal equivalent circuit diagram 510 of

25 **figure 5B** shows a controlled current source $g_m(\Delta V_G - \Delta V_{out})$ 511 and also an internal resistance g_{ds}. In accordance with the small-signal equivalent circuit diagram 510 shown in figure 5B, the field-effect-based modulation of the electric current at the lower source/drain

30 terminal of the MOS transistor 401 in accordance with figure 5A is represented as controlled current source $g_m(\Delta V_G - V_{out})$ 511.

The dependence of said electric current on the

35 electrical voltage at the lower source/drain terminal of the MOS transistor 401 in accordance with figure 5A is determined by the conductance g_{ds}. The time constant τ_c of the amplifier is determined by the RC element and

is described by the following expression:

$$\tau_c = C/(g_{ds} + g_m) \qquad (3)$$

5   The time constant τ_c from equation (3) corresponds to
the scenario of the common-source connection of the MOS
transistor 401 from figure 4A if the value of the
nonreactive resistance R is equal to the inverse
transconductance g_m^{-1} of the MOS transistor 401 (cf.
10   equation (2)). In accordance with the two circuit
architectures, the gain is then approximately one,
namely:

$$A(\omega = 0) = \Delta V_{out}/\Delta V_G = g_m/(g_m + g_{ds}) \leq 1 \qquad (4)$$

15
This low gain is disadvantageous, on account of the
small signal amplitudes that have to be conducted out
from the sensor device, since noise effects can corrupt
the measured signal.
20
As an example of a realization of the principle
described on the basis of a CMOS camera, reference
shall be made to [1].

25   To summarize, the functionality of the circuit
architectures disclosed in the prior art for reading
out sensor signals of a sensor array is inadequate
since a large time constant for reading the individual
sensor devices results from the capacitance that is to
30   be subjected to charge reversal. This leads to a poor
temporal resolution. Furthermore, the gain of the often
small sensor signal is often insufficient in the case
of circuit architectures disclosed in the prior art.

35   The invention is based on the problem of providing a
sensor arrangement having high spatial resolution
which, in conjunction with a sufficiently high signal
gain, enables a fast read-out of sensor signals, i.e. a

high bandwidth.

The problem is solved by means of a sensor arrangement
and by means of a method for operating a sensor
arrangement having the features in accordance with the
independent patent claims.

The sensor arrangement according to the invention
contains a plurality of sensor devices formed on and/or
in a substrate. Each sensor device has an electrical
signal converter and a sensor element coupled to the
signal converter, which sensor element can be used to
characteristically influence the electrical
conductivity of the signal converter on account of a
sensor event on the sensor element. Furthermore, the
sensor device according to the invention has a device
for keeping constant an electrical voltage present at
the signal converter. Moreover, each sensor device has
a device for detecting the value of the electric
current flowing through the signal converter as sensor
signal.

Furthermore, the invention provides a method for
operating a sensor arrangement having the features
mentioned above, in which case, in accordance with the
method, the electrical conductivity of the signal
converter is characteristically influenced on account
of a sensor event on a respective sensor element.
Furthermore, the electrical voltage at the signal
converter is kept constant. The electric current
flowing through the signal converter is detected as
sensor signal.

A fundamental idea of the invention is based on
detecting, instead of the electrical voltage, an
electric current at a signal converter coupled to the
sensor element. By virtue of an electric current being
detected according to the invention, rather than an

electrical voltage in accordance with the prior art, a
charge reversal of capacitances is avoided. A larger
bandwidth, that is to say a faster read-out of the
sensor elements of a sensor arrangement, is made
5   possible as a result. The time constant of the system
is no longer defined by the interconnection within the
sensor device, but rather only by the external circuit.
Clearly, the electrical voltage as sensor signal is
stabilized externally according to the invention. With
10   the circuit architecture according to the invention for
a sensor arrangement, a particularly high number of
sensor elements and a particularly high sampling rate
are made possible for a predetermined technology,
thereby achieving a small time constant for reading the
15   sensor elements. On account of the interconnection of
the sensor device according to the invention, an
electric sensor current is detected instead of an
electrical sensor voltage, which leads to a high gain
and a small time delay.

20

If, instead of the electrical voltage V_{out}, the electric
current I_{out} is used as output variable of the output
stage of a sensor device or of the signal converter,
then the voltage across the capacitance becomes
25   independent of the output variable and can be kept
constant at a value of the output voltage, by way of
example. Since the inductive properties of integrated
leads are generally negligible compared with the
capacitive properties, this results in a considerably
30   reduced time constant. In practice, an unavoidable
internal resistance of the measuring circuit leads to a
small voltage drop. However, since the measuring
circuit is situated outside the sensor devices, its
internal resistance can be kept down. As a result, the
35   time constant $\tau = RC$ is orders of magnitude smaller
than in accordance with the prior art. Sensor
arrangements that can be read faster or an increased
number of sensor devices are made possible as a result.

Clearly, an output driver circuit of a sensor device is embodied in a "current mode technology".

5   A further important aspect of the invention is to be seen in the fact that a plurality of sensor devices are formed on and/or in the substrate. In other words, the sensor arrangement according to the invention is realized as an integrated circuit, for example in

10   and/or on a silicon substrate (e.g. wafer, chip, etc.). Miniaturization is achieved as a result and an array having a high number of sensor devices is thus produced. Furthermore, the sensor arrangement can be fabricated with tenable outlay using the modern and

15   mature silicon microtechnology.

Preferred developments of the invention emerge from the dependent claims.

20   In the case of the sensor arrangement, the electronic signal converter is preferably a transistor (e.g. a bipolar transistor).

In at least some of the sensor devices according to the

25   invention, the electronic signal converter may be a field-effect transistor whose gate terminal is coupled to the sensor element, the device for keeping constant an electrical voltage being set up in such a way that it keeps constant the electrical voltage between the

30   source/drain terminals of the field-effect transistor. A field-effect transistor as signal converter has the functionality that a modulation of the gate voltage is converted into an altered electrical conductivity of the channel region of the field-effect transistor, so

35   that the value of the electric current flowing through a source/drain terminal is characteristically influenced on account of the altered nonreactive resistance of the channel region of the field-effect

transistor.

As an alternative to a field-effect transistor, the electronic signal converter may be embodied as an arbitrarily configured controllable nonreactive resistor, for example as a potentiometer, the resistance of which is controlled for example by means of an electrical signal on account of a sensor event.

Furthermore, the sensor device according to the invention may have an evaluation unit, the evaluation unit being provided with the value of the electric current as sensor signal.

The evaluation unit is preferably set up in such a way that it forms, from the value of the electric current, an electrical voltage characteristic of this value or maps the value of the electric current onto a digitally coded value that characterizes the latter.

In other words, the detected electric current can be converted into an electrical voltage, which may be advantageous for the further processing of the signal. Furthermore, an analog current signal can be converted into a digital signal - and hence a signal that is more robust in respect of errors.

In particular, the evaluation unit may have an operational amplifier, in particular connected up as a voltage follower, having a first input, to which the sensor signal can be applied. Furthermore, the operational amplifier has a second input, to which an electrical reference potential can be applied. The characteristic electrical voltage is provided at an output of the operational amplifier, the first input and the output being coupled to one another by means of a nonreactive resistor.

The sensor arrangement may be configured as a biosensor arrangement. The sensor element of each sensor device may for example detect an electrical signal of a nerve cell grown on the sensor element. As an alternative,
5   the sensor element may detect electrically charged particles on the sensor element using an ISFET.

The sensor arrangement may have a calibration device for calibrating a respective sensor device, which is
10 set up in such a way that it can be used to bring the gate region of the field-effect transistor to an electrical calibration potential such that the electric current is independent of parameter fluctuations of the field-effect transistor. By way of example, field-
15 effect transistors of different sensor devices may have different parameters (e.g. threshold voltage) due to a fabrication method. The calibration makes it possible to ensure that parameter fluctuations do not lead to corruption in the detection of a sensor event.
20
In particular, the sensor device can be calibrated by means of implementing a calibration device based on the autozeroing technique, thereby providing a robust sensor arrangement. A signal influencing on account of
25 parameter fluctuations of the components of a respective sensor device, for example the signal converters realized as field-effect transistors, is thereby avoided.

30 The calibration device may be set up in such a way that an electric calibration current can be applied to the gate terminal and to a source/drain terminal of the field-effect transistor for calibration purposes.

35 As an alternative, the evaluation unit may have a correlated double sampling device, which may be set up in such a way that it forms, in the case of a sensor event, a value of the electric current that is

independent of parameter fluctuations of a respective field-effect transistor.

In accordance with the correlated double sampling
5   principle, clearly in a first step a sensor event is detected in a sensor device and the sensor signal is stored. This sensor signal is dependent on the alteration of the value of the physical parameters of the sensor device (for example geometrical parameters
10   of a field-effect transistor) and may furthermore be dependent on physical parameters of further components, for example an amplifier for amplifying the sensor signal. In a second step, an auxiliary signal that depends only on the value of the physical parameter of
15   the sensor device is detected in the absence of a sensor event. If the auxiliary signal is subtracted from the sensor signal, then a sensor signal that is essentially independent of the value of the physical parameter is obtained.
20

In particular, the correlated double sampling device of the invention may be set up in such a way that, by means of this device, in a calibration phase, the gate region of the field-effect transistor is brought to an
25   electrical calibration potential and the associated value of the electric current is detected as calibration signal and stored. In a detection phase, the value of the electric current on account of a sensor event is detected as sensor signal. In an
30   evaluation phase, sensor signal and calibration signal can be evaluated jointly.

Preferably, the sensor devices of the sensor arrangement are arranged essentially in matrix form on
35   and/or in the substrate and are connected up by means of row and column lines in such a way that the sensor devices can be driven individually, row by row or column by column.

In the case of the sensor arrangement according to the invention, at least one evaluation unit, at least one calibration device and/or at least one correlated double sampling device may be provided jointly for at least a portion of the sensor devices of a row line or a column line.

The method according to the invention for operating the sensor arrangement according to the invention is described in more detail below. Refinements of the sensor arrangement are also applicable to the method for operating the sensor arrangement, and vice versa.

In accordance with the method according to the invention, a field-effect transistor whose gate terminal is coupled to the sensor element may be used as the electronic signal converter of a respective sensor arrangement, the electrical voltage between the source/drain terminals of the field-effect transistor being kept constant by means of the device for keeping constant an electrical voltage.

Furthermore, a respective sensor device may be calibrated by the gate region of the field-effect transistor being brought to an electrical calibration potential such that the value of the electric current in the case of a sensor event becomes independent of the properties of the field-effect transistor (e.g. a production-dictated deviation of the thickness of the gate insulating layer from a desired or average value).

A value of the electric current that is independent of the properties of the field-effect transistor may be formed using the correlated double sampling method in the case of a sensor event.

Exemplary embodiments of the invention are illustrated

in the figures and are explained in more detail below.

In the figures:

5   figure 1   shows   an   illustration   of   one   sensor
             arrangement in accordance with the prior art,

    figure 2   shows   an   illustration   of   another   sensor
             arrangement in accordance with the prior art,

10
    figure 3   shows a diagram illustrating a signal profile
             as a function of a read-out time,

    figure 4A, figure 4B show one output driver circuit and
15   an associated small-signal equivalent circuit
             diagram in accordance with the prior art,

    figure 5A, figure 5B show another output driver circuit
             and   an   associated   small-signal   equivalent
20   circuit diagram in accordance with the prior
             art,

    figure 6   shows a sensor device in accordance with a
             preferred   exemplary   embodiment   of   the
25   invention,

    figure 7   shows an evaluation unit according to the
             invention,

30 figure 8   shows a sensor arrangement in accordance with
             a   first   exemplary   embodiment   of   the
             invention,

    figure 9   shows a sensor arrangement in accordance with
35   a   second   exemplary   embodiment   of   the
             invention,

    figure 10 shows a sensor arrangement in accordance with

a third exemplary embodiment of the invention.

A description is given below, referring to **figure 6**, of a sensor device 600 in accordance with a preferred exemplary embodiment of the invention.

The sensor device 600 shown in figure 6 has a field-effect transistor 601 as electrical signal converter. Furthermore, the sensor device 600 has a biosensor element coupled to the field-effect transistor 601, which biosensor element is represented schematically as voltage source 602 in figure 6. If a sensor event takes place at the biosensor element, then the electrical conductivity of the channel region of the field-effect transistor 601 is characteristically influenced on account of said sensor event.

A first source/drain terminal 601a of the field-effect transistor 601 is coupled to one terminal of an ammeter 603 for detecting a sensor current I_{out}, a supply voltage 604 being applied to the other terminal of said ammeter. A second source/drain terminal 601b of the field-effect transistor 601 is at the ground potential 605. On account of this interconnection, a constant electrical potential difference is applied between the source/drain terminals 601a, 601b. Furthermore, the constant voltage V_{out}, which results from the difference between the supply voltage 604 and the ground potential 605, is also present across a capacitor 606 representing the effective capacitance of the sensor device 600. The ammeter 603 is a device for detecting the value of the electric current flowing through the first source/drain terminal 601a of the field-effect transistor 601 as sensor signal.

The gate terminal 601c of the field-effect transistor 601 is coupled to the voltage source 602. The

electrical voltage between the source/drain terminals 601a, 601b of the field-effect transistor 601 is constant. The first source/drain terminal 601a of the field-effect transistor 601 is coupled to one terminal
5   of the capacitor 606 and is furthermore coupled to the ammeter 603.

If a sensor event takes place on the biosensor element, then the electrical voltage V_G of the voltage source
10 602 is thereby modulated. The latter is provided at the gate terminal 601c of the field-effect transistor 601, so that the electrical conductivity of the channel region of the field-effect transistor 601 is thereby characteristically influenced. As a result, the value
15 of the electric current flow through the source/drain terminal 601a of the field-effect transistor 601, which current flow is detected by the ammeter 603, is a characteristic measure of the sensor event.

20 The field-effect transistor 601 is operated in the "current mode". The voltage source 602 V_G determines the potential present at the gate region 601c, whereas the voltage at the first source/drain terminal 601a is fixed at the supply voltage 604. The output current I_{out}
25 is detected by means of the ammeter 603. It should be noted that the capacitance C 606 does not have to be subjected to charge reversal since the voltage is kept constant.

30 A description is given below, referring to **figure 7**, of an evaluation unit 700 in accordance with a preferred exemplary embodiment of the invention.

The evaluation unit has the functionality of keeping
35 constant the electrical voltage on a sensor line and of simultaneously converting the detected sensor current (preferably linearly) into a sensor voltage. This enables further processing in the voltage domain.

For some applications it may be advantageous for a detected electric sensor current to be converted into a voltage signal. The evaluation unit 700 shown in figure 7 shows an exemplary embodiment that enables a current signal ΔI_{meas} to be converted into a voltage signal ΔV_{out}. The circuit shown in figure 7 is used both to keep constant the electrical voltage on the line and to convert the modulated current I_{meas} into a modulated output voltage $V_{out} = I_{meas}Z$. In this case, Z denotes the value of an impedance 701.

As shown in figure 7, the modulated value of the electric current ΔI_{meas} is provided as sensor signal at an input 702 of the evaluation unit 700. The evaluation unit 700 has an operational amplifier 703. The operational amplifier 703 has a noninverting input 703a, at which the sensor signal ΔI_{meas} is provided. Furthermore, the operational amplifier 703 has a noninverting input 703b, to which a constant electrical reference potential V_{kal} is applied. The characteristic electrical voltage ΔV_{out} is provided at an output 703c of the operational amplifier 703. The output 703c of the operational amplifier 703 is fed back to the inverting input 703a of the operational amplifier 703 via the impedance Z 701. As is furthermore shown in figure 7, the electrical potential V_{kal} at the noninverting input 703b of the operational amplifier 703 is provided by means of the constant-voltage source 704. The constant-voltage source 704 is connected between the electrical ground potential 605 and the noninverting input 703b of the operational amplifier 703.

A description is given below, referring to figure 8, of a sensor arrangement 800 in accordance with a first preferred exemplary embodiment of the invention.

The sensor arrangement 800 has a multiplicity of sensor devices 801 which are arranged in matrix form and are connected up by means of row and column lines in such a way that the sensor devices 801 can be driven
5   individually or column by column.

The sensor devices 801 of the sensor arrangement 800 are formed on and in a silicon substrate (not shown). In other words, the sensor arrangement 800 is realized
10   as an integrated circuit.

Although the sensor arrangement 800 has a multiplicity of sensor devices 801, only the n-th and (n+1)-th column of sensor devices 801 and also the m-th and
15   (m+1)-th row of sensor devices 801 are shown in figure 8 for the purpose of a simplified illustration.

The construction of the sensor device 801 arranged in the n-th column and the m-th row from figure 8 is
20   described in more detail by way of example below.

A sensor element 801 of the sensor arrangement 800 is shown schematically as voltage source 802 in fig. 8, said sensor element being arranged between the ground
25   potential 605 and one terminal of a capacitor 803. The capacitor 803 symbolizes a dielectric which is applied on the sensor element and spatially decouples electrically charged particles to be detected that are situated thereon from the gate region 804c of a
30   detection transistor 804. The other terminal of the capacitor 803 is furthermore coupled to the first source/drain terminal 805a of a calibration transistor 805. The second source/drain terminal 805b of the calibration transistor 805 is coupled to the first
35   source/drain terminal 804a of the detection transistor 804. Furthermore, the first source/drain terminal 804a of the detection transistor 804 is coupled to the first source/drain terminal 806a of a selection transistor

806. The second source/drain terminal 806b of the selection transistor 806 is coupled to a changeover element 807, which is provided jointly for each row of sensor devices 801. The gate terminal 806c of the
5   selection transistor 806 is coupled to a first column line 808, which is provided jointly for each column of sensor devices 801. The second source/drain terminal 804b of the detection transistor 804 is coupled to a row line 809, which is provided jointly for each row of
10 sensor devices 801. The changeover element 807 can be switched in one of two switch positions "a" and "b", depending on whether a calibration mode or a measurement mode is to be set. In accordance with the scenario shown in fig. 8, the switch element 807 is in
15 the position "b", so that the second source/drain terminal 806b of the selection transistor 806 is coupled to a calibration constant-current source 810. By contrast, if the changeover element 807 is in the switch position "a" (not shown in the figure), then the
20 second source/drain terminal 806b of the selection transistor 806 is coupled to a detection constant-voltage source 811. The value of the electric current flowing on the row line 809 can be detected by means of a current detection unit 812, i.e. an ammeter for
25 example.

Furthermore, a selection terminal 813 is coupled to the first column line 808. If an electrical signal having a logic value "1" is applied to the selection terminal
30 813, then all the selection transistors 806 of the associated column of sensor devices 801 are electrically conductive, so that the associated column of sensor devices 801c is selected. Furthermore, a calibration terminal 814 is in each case coupled to a
35 respective second column line 815, a common second column line 815 and a common calibration terminal 814 being provided for each column of sensor devices 801. If a signal having a logic value "1" is present at the

calibration terminal 814, then all the calibration
transistors 805 of the associated column of sensor
devices 801 are electrically conductive, thereby
enabling calibration.

The functionality of the sensor arrangement 800 is
described in more detail below.

Firstly, a description is given of how the sensor
devices 801 are calibrated column by column in order to
compensate for fluctuating properties between different
sensor devices (for example fluctuations in the value
of the threshold voltage of the detection transistors
804). In order to calibrate the n-th column, the latter
is activated as sole column by a control signal having
a logic value "1" being applied to the selection
terminal 813 of the n-th column of sensor devices 801.
A signal having a logic value "0" is present at the
selection terminals 813 of all the other columns of
sensor devices 801. As a result, the channel regions of
all the selection transistors 806 of the n-th column of
sensor devices 801 are electrically conductive, whereas
the selection transistors 806 of all the other columns
of sensor devices 801 are nonconductive. A read-out or
calibration circuit with the changeover element 807 is
in each case situated outside each row of sensor
devices 801. In order to carry out the calibration, the
switch is brought to the position "b". This scenario is
shown in fig. 8. For calibration, a signal having a
logic value "1" is momentarily applied to the
calibration terminal 814 of the n-th column of sensor
devices 801, so that the calibration constant-current
source 810 is coupled to the gate terminal 804c of the
detection transistor 804 via the conductive selection
transistor 806 and the conductive calibration
transistor 805. As a result, a constant current I_{kal} is
impressed into the sensor device 801. If the
calibration transistor 805 is in the on state, then

exactly the electrical voltage required to derive the electric current I_{kal} through the detection transistor 804 is established at the gate terminal 804c of the detection transistor 804. This voltage is different for each sensor device 801 of the n-th column of sensor devices 801 since the electrical parameters of the detection transistor 804 may vary on account of statistical effects. If the coupling of the gate terminal 804c and the first source/drain terminal 804a of the detection transistor 804 via the calibration transistor 805 is interrupted again by the signal at the calibration terminal 814 being brought to a logic value "0", clearly the electrical gate voltage associated with the electric current value I_{kal} is stored at the gate terminal 804c of the detection transistor 804. This calibration method is gradually repeated for all the columns.

A measurement phase of the sensor arrangement 800 is described below.

For this purpose, the changeover element 807 is switched to the switch position "a" (not shown in figure 8). As a result, the constant voltage V_{drain} is impressed into all the circuit devices 801 of an associated row of circuit devices 801 using the detection constant-voltage source 811. The sensor arrangement 800 is sequentially read column by column. A column to be read is selected by the associated selection terminal 813 being brought to an electrical potential with a logic value "1", so that all the selection transistors 806 of the associated column of sensor arrangements 801 are brought to an electrically conductive state. If no sensor event takes place at a sensor element of a sensor device 801 of a selected column of sensor devices 801, then that DC component that was stored on the gate terminal 804c of the detection transistor 804 in the calibration phase flows

through the activated sensor device 801. Parameter
fluctuations, in particular of the detection
transistors 804, are therefore compensated for. In
other words, the output signal for an identical sensor
5   event is identical and does not depend on the
fluctuating parameters of the transistors. If a sensor
event gives rise to a modulation of the electrical
potential on a sensor element, then this results in a
modulation of the electrical voltage at the gate
10 terminal 804c of the associated detection transistor
804 and consequently of the electric current at the
first source/drain terminal 804a of the detection
transistor 804. This modulation is detected by means of
the current detection unit 812 and can be amplified by
15 external amplifier elements. The electric sensor
current signal may optionally be converted into an
electrical voltage (cf. evaluation unit 700 from figure
7).

20 To summarize, it shall be emphasized that the sensor
devices 801 can be activated and deactivated column by
column by means of the sensor arrangement 800. A sensor
signal is amplified or converted into an electric
current. Statistical fluctuations of parameters of the
25 sensor devices 801 are compensated for by means of
calibrating the sensor devices 801.

A description is given below, referring to **figure 9**, of
a sensor arrangement 900 in accordance with a second
30 preferred exemplary embodiment of the invention. The
sensor arrangement 900 shown in Figure 9 is a
modification of the sensor arrangement 800 shown in
figure 8. Identical or similar components are therefore
provided with the same reference numerals.

35

The essential difference between the sensor arrangement
900 and the sensor arrangement 800 is that the
calibration transistor 805 is connected up in a

modified manner in the case of the sensor devices 901
of the sensor arrangement 900.

In the case of the sensor arrangement 900, the second
5   source/drain   terminal   805b   of   the   calibration
transistor 805 is coupled to the second source/drain
terminal 806b of the selection transistor 806 and
directly to the row line 809. By virtue of the
calibration transistor 805 of the sensor arrangement
10 900 being directly coupled to the row line 809 (clearly
read-out line), it is possible to compensate for slight
fluctuations   which   may   arise   via   the   selection
transistor 806. However, the parasitic capacitance at
the output node of a sensor arrangement 901 in
15 accordance with the sensor arrangement 900 may be
somewhat higher since, in this case, two transistors
are   permanently   connected   by   their   source/drain
terminals to the common output node of a sensor
arrangement 901 of a row.
20

A description is given below, referring to **figure 10**,
of a sensor arrangement 1000 in accordance with a third
preferred exemplary embodiment of the invention. Those
components of the sensor arrangement 1000 which also
25 occur in the sensor arrangement 800 or 900 are provided
with the same reference numerals.

The   sensor   arrangement   1000   is   a   matrix-type
arrangement of a multiplicity of sensor devices 1005.
30

A sensor element of a sensor device 1005 is again
symbolized as voltage source 802, which, in accordance
with figure 10, are connected between a terminal at
electrical ground potential and the capacitor 803. The
35 capacitor 803 represents a dielectric layer on the
detection transistor 804, by means of which the sensor
element 802 is decoupled from the detection transistor
804. The capacitor 803 is coupled to the first

source/drain terminal 1001a of a switching transistor 1001. The second source/drain terminal 1001b of the switching transistor 1001 is coupled to the first source/drain terminal 805a of the calibration

5   transistor 805 and to the gate terminal 804c of the detection transistor 804. Furthermore, the gate terminal 1001c of the switching transistor 1001 is coupled to a switching terminal 1002 via a third column line 1003. A separate third column line 1003 is

10 provided for each column of sensor devices 1005. The first source/drain terminal 804a of the detection transistor 804 is coupled to the first source/drain terminal 806a of the selection transistor 806, the gate terminal 806b of which is coupled to the selection

15 terminal 813 via the first column line 808. The gate terminal 805c of the calibration transistor 805 is coupled to the calibration terminal 814 via the second column line 815. The second source/drain terminal 805b of the calibration transistor 805 is coupled to a first

20 row line 1006, which is provided jointly for each row of sensor devices 1005. The first row line 1006 is coupled to a calibration constant-voltage source 1004. The second source/drain terminal 806b of the selection transistor 806 is coupled via a second row line 1007 to

25 the detection constant-voltage source 811, which is in turn coupled to the current detection unit 812. The current detection unit 812 is coupled to the calibration constant-voltage source 1004.

30 The functionality of the sensor arrangement 1000 is described in more detail below.

In the case of the sensor arrangement 1000, the sensor devices 1005 can be activated and deactivated column by

35 column. The sensor signal or a reference signal can be amplified or converted into an electric current. Furthermore, the sensor device 1000 is suitable for a correlated double sampling for the purpose of

eliminating parameter fluctuations.

It should be noted that the n-MOS transistors 1001, 805, 806 coupled to one of the column lines 1003, 815
5   and 808, respectively, can be brought to an electrically conductive state by application of an electrical signal having a logic value "1" to the associated terminal 1002, 814 and 813, respectively, and thus represent a negligibly small nonreactive
10   resistance. By contrast, if the electrical signal at an associated terminal 1002, 814 and 813, respectively, is at a logic value "0", then the driven transistor is in the off state, in which case the leakage currents of the field-effect transistors can be disregarded.
15

The sensor arrangement 1000 is based on the correlated double sampling principle (CDS), whereby parameter fluctuations and low-frequency noise are suppressed. In accordance with the CDS method, it is customary firstly
20   to apply a reference signal to an input of an amplifier. The amplified reference signal plus an offset signal of the amplifier is then stored at the output of the amplifier. In a next phase, the sensor signal is applied to the amplifier. The amplified
25   measurement signal including the offset signal is then present at the output of the amplifier. Forming the difference between the two values makes it possible to eliminate the offset signal of the amplifier.

30   The sensor devices 1005 of the sensor arrangement 1000 are sequentially read column by column. A column (e.g. the n-th column) of sensor devices 1005 is in each case activated by the selection terminal 813, the first column line 808 and consequently the gate terminal 806c
35   of the selection transistors 806 of the associated column being brought to a logic value "1". The pixels of a column are read in two phases in accordance with the exemplary embodiment.

In a first phase, the reference voltage V_{kal} of the
calibration   constant-voltage   source   1004,   in   an
associated sensor arrangement 1005, is converted into

5   an electric current and the value thereof is detected.
For this purpose, an electrical signal having a logic
value "1" is applied to the calibration terminal 814,
so that the calibration transistors 805 coupled thereto
via the second column line 815 are brought to an

10   electrically   conductive   state.   By   contrast,   the
switching terminal 1002 is at a logic value "0" in this
phase,   so   that   the   switching   transistor   1001   is
electrically nonconductive. The reference voltage V_{kal}
is present at the gate terminal 804c of the detection

15   transistor 804, which results in an associated electric
current through the first source/drain terminal 804a of
the   detection   transistor   804.   The   value   of   said
electric current may be different for different sensor
devices 1005 of the sensor arrangement 1000 on account

20   of statistic fluctuations of transistor parameters. The
value of said electric current is detected and stored
in the read-out circuit of the respective row as
electric reference current $I_{meas}(m)$.

25   The actual sensor signal is detected in a second phase.
In a shortest possible time interval with respect to
the   first   phase,   the   electrical   signal   at   the
calibration terminal 814 is brought to a logic value
"0" as a result of which the calibration transistors

30   805 turn off. By contrast, an electrical signal having
a logic value "1" is applied to the switching terminal
1002,   so   that   the   switching   transistors   1001   are
brought   to   an   electrically   conductive   state.   As   a
result,   a   change   in   the   electrical   potential   at   the

35   sensor element 802 is mapped on the gate terminal 804c
of   the   detection   transistor   804,   which   leads   to   a
modulation of the electric current through the first
source/drain terminal 804a of the detection transistor

804. The value of said electric current is detected, and the difference between the detected current values from the first and the second phase is then formed. As a result, parameter fluctuations between the different sensor devices are suppressed and the output signal obtained depends exclusively on the sensor event.

The following publication is cited in this document:

[1]   Stevanovic, N., Hillebrand, M., Hosticka, B.J.,
      Teuner, A. (2000) "A CMOS Image Sensor for High-
      Speed Imaging", IEEE International Solid-State
      Circuits Conference 2000:104-105

List of reference symbols

100	Sensor arrangement
101	First sensor device
102	Second sensor device
103	Third sensor device
104	Fourth sensor device
105	Multiplexer
106	Read-out circuit
200	Sensor arrangement
201	Nonreactive resistance
202	Capacitance
300	Diagram
301	Abscissa
302	Ordinate
303	Signal profile curve
400	Output driver circuit
401	MOS transistor
402	Voltage source
403	Constant-current source
404	Nonreactive resistance
405	Capacitance
406	Supply voltage
407	Ground potential
410	Equivalent circuit diagram
411	Controlled current source
412	Internal resistance
500	Output driver circuit
510	Equivalent circuit diagram
511	Controlled current source
512	Internal resistance
600	Sensor device
601	Field-effect transistor
601a	First source/drain terminal
601b	Second source/drain terminal
601c	Gate terminal
602	Voltage source
603	Ammeter

604	Supply voltage
605	Ground potential
606	Capacitor
700	Evaluation unit
701	Impedance
702	Input
703	Operational amplifier
703a	Inverting input
703b	Noninverting input
703c	Output
704	Constant-voltage source
800	Sensor arrangement
801	Sensor device
802	Voltage source
803	Capacitor
804	Detection transistor
804a	First source/drain terminal
804b	Second source/drain terminal
804c	Gate terminal
805	Calibration transistor
805a	First source/drain terminal
805b	Second source/drain terminal
805c	Gate terminal
806	Selection transistor
806a	First source/drain terminal
806b	Second source/drain terminal
806c	Gate terminal
807	Changeover element
808	First column line
809	Row line
810	Calibration constant-current source
811	Detection constant-voltage source
812	Current detection unit
813	Selection terminal
814	Calibration terminal
815	Second column line
900	Sensor arrangement
901	Sensor device

1000   Sensor arrangement
1001   Switching transistor
1001a   First source/drain terminal
1001b   Second source/drain terminal
1001c   Gate terminal
1002   Switching terminal
1003   Third column line
1004   Calibration constant-voltage source
1005   Sensor device
1006   First row line
1007   Second row line